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Study of Stability Diagrams of Codoped Silicon Nano-Transistors

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This study provides insights into the behavior of nanoscale silicon-on-insulator transistor with codoped channels, in particular at low temperatures. The goal is to compare the stability diagrams (plots of current as a function of gate voltage and source-drain bias) for several devices fabricated in the same batch, but having different designed channel widths. For the narrower device, a simple stability diagram containing a small number of Coulomb diamonds is observed, while for the wider device, a relatively more complex set of overlapped Coulomb diamonds indicates the presence of a larger number of quantum dots. Here, it is also shown how applying a vertical electric field by using the substrate voltage can significantly change the current paths in such devices.

topics: single-electron transistor, silicon-on-insulator, Coulomb blockade, stability diagram

1. Introduction

Silicon (Si) transistors have been the backbone of the electronics industry for many decades, being continuously miniaturized into single-digit-nm dimensions according to Moore's law [1]. At the same time, the impact of individual (discrete) impurities (dopants) — necessary to modulate the conductivity of Si — is becoming more and more critical, since the number and positions of the dopants dramatically affect the threshold voltage of the transistors [2–4]. Controlling the dopant distribution by techniques such as single ion implantation (SII) [5] or atomic manipulation by scanning tunneling microscopy (STM) [6, 7] can provide more control of the electrical characteristics, although these techniques are too sophisticated for large-scale integration. Furthermore, single-electron tunneling through dopants as quantum dots (QDs) has been reported in several papers [8–10].

An alternative to conventional npn or pnp transistor designs emerged with the development and demonstration of junctionless transistors (JLTs) [11, 12]. In such devices, doping with impurities (dopants) is performed at high concentrations throughout the device, including the source/drain lead extensions and the channel area, which should be designed as a nanowire so that the gate can sufficiently control its potential to switch the device on or off. In our laboratory, we have demonstrated that in such junctionless transistors doped in different regimes of concentrations, quantum dots (QDs) formed by either individual dopants (for relatively low concentrations) or by clusters of dopants (for relatively high concentrations) can be formed to conduct current by single-electron tunneling (SET) [13–17]. More recently, we demonstrated that even when the doping concentration is raised to 10^{19} cm^{-3} or even above 10^{20} cm^{-3}, SET transport can still dominate the current, not only at low temperature (as usually reported) but also near room temperature [18, 19]. This is due to a combination of factors, such as sufficiently high doping concentration to ensure low resistance in the nearby leads but at the same time sufficiently small channels to leverage the dopant randomness to statistically obtain cluster-dopant QDs. The demonstration of SET operation for a small number of devices at temperatures near room temperature is promising for the development of practical applications of SET transport.

Additional capabilities can be gained by codoping the devices, in our case the top layer of a silicon-on-insulator (SOI) wafer. Codoping in the fabrication of the devices presented in this study is done by first doping phosphorus (P) donors at high concentration, followed by counter-doping with boron

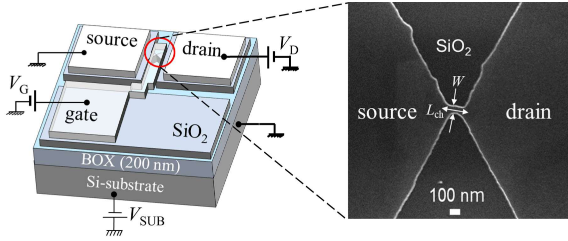

Fig. 1. Schematic device structure of a SOI transistor, also indicating the biasing circuit. The channel is shown zoomed-in on the right by an SEM image of one of the narrowest devices available in this batch.

(B) acceptors at somewhat lower concentration. In such structures, it is expected that the P-donors are still responsible for the formation of cluster-dopant QDs, but the B-acceptors in the background assist by compensating a number of P-donors, thus enhancing the probability of finding donor-induced QDs [20]. It can be also expected that higher tunnel barriers can be obtained in such systems, in which B-acceptors intercalated between P-donor-induced QDs can locally enhance the potential [21]; more study is needed to clarify this issue.

In this study, we utilize codoped SOI-field-effect transistors (FETs) to study the SET behavior, in particular at low temperatures and as a function of channel width. For this, we focus on the analysis of two devices (SOI-FETs) in terms of stability diagrams that reflect the properties of the SET transport based on the Coulomb blockade.

2. Device structure and experimental results

2.1. Device fabrication and parameters

As shown in Fig. 1, the devices studied in this work are SOI-FETs with the top Si layer having a thickness of about 18 nm at the end of the processing. The doping is performed in two steps, first with P-donors and second with B-acceptors, at drive-in temperatures and times of 860°C and 20 min for P-doping, respectively, and 960°C 5 min for B-doping, resulting in the concentrations: $N_D \approx 2.0 \times 10^{20}$ cm^{-3} and $N_A \approx 0.5 \times 10^{20}$ cm^{-3}. Nano-patterning was subsequently done using an electron-beam lithography technique, with the channel length (L) and width (W) as parameters. The gate oxide has been thermally grown as $t_{ox} \approx 10 \pm 1$ nm. Then, the electrodes are defined by a lift-off process in Al, with a thickness of about 250 nm.

It should be noted that the nano-patterning process and the thermal oxidation for the gate-oxide formation may change the effective doping concentration due to phenomena such as segregation or aggregation. These phenomena affect P-donors and B-acceptors differently, potentially leading to modifications of dopant distribution near the interfaces.

For comparison, in this study we focus on SOI-FETs with $L = 0$ nm (point-contact devices), but with different designed widths ($W = 60$ nm and $W = 200$ nm). A typical scanning electron microscope (SEM) image of such a device is shown in the inset in Fig. 1. The usual bias circuit is also illustrated in Fig. 1. The temperature of all measurements described in this work is 8.0 ± 0.1 K.

2.2. Experimental results

A typical measurement that can most clearly reveal the SET transport properties is the so-called stability diagram, i.e., a plot of $|I_D|$ in the V_G–V_D plane. When combined with the I_D–V_G characteristics, stability diagrams can allow the evaluation of the number of electrons injected in the channel's QDs, but also the degree of complexity of the QD array carrying the SET current. In addition, the effect of the vertical electric field can be monitored by applying both V_G (top-gate voltage) and V_{SUB} (substrate voltage working as back-gate voltage).

Figure 2 shows the stability diagrams for the narrowest device under study, a SOI-FET with designed dimensions $L = 0$ nm and $W = 60$ nm, at two different V_{SUB} (0 V and −8 V). Distinct Coulomb diamonds can be observed for this device, suggesting that a single QD dominates the SET transport. Dashed lines mark the edges of the diamonds observed for $V_{SUB} = 0$ V and are also transferred to the stability diagram observed for $V_{SUB} = -8$ V. a relatively small but clear shift to the right (i.e., more positive V_G values) is noticeable, along with the emergence of small new Coulomb diamonds. The shift is smaller than expected when we consider only the parallel-plate capacitance models with $t_{ox} \approx 10$ nm (for the top-gate oxide) and $t_{BOX} \approx 200$ nm (for the buried oxide). This can be ascribed to the fact that the channel may be suspended in this case due to significant underetching, thus having a vacuum replacing the buried oxide underneath the channel, at least partly.

The shift can be systematically observed from the I_D-V_G characteristics measured for several different V_{SUB} values, also shown in Fig. 2. The simple behavior suggests that this narrow and thin channel can only accommodate a dominant QD, giving rise to a simple set of Coulomb diamonds as electrons are added one by one to the quantum dot.

On the other hand, the behavior observed for a wider device, with designed dimensions $L = 0$ nm and $W = 200$ nm, is significantly different, as shown in Fig. 3. First of all, a much more complex set of Coulomb diamonds is observed, with most of the diamonds overlapping each other and with the diamond height oscillating in

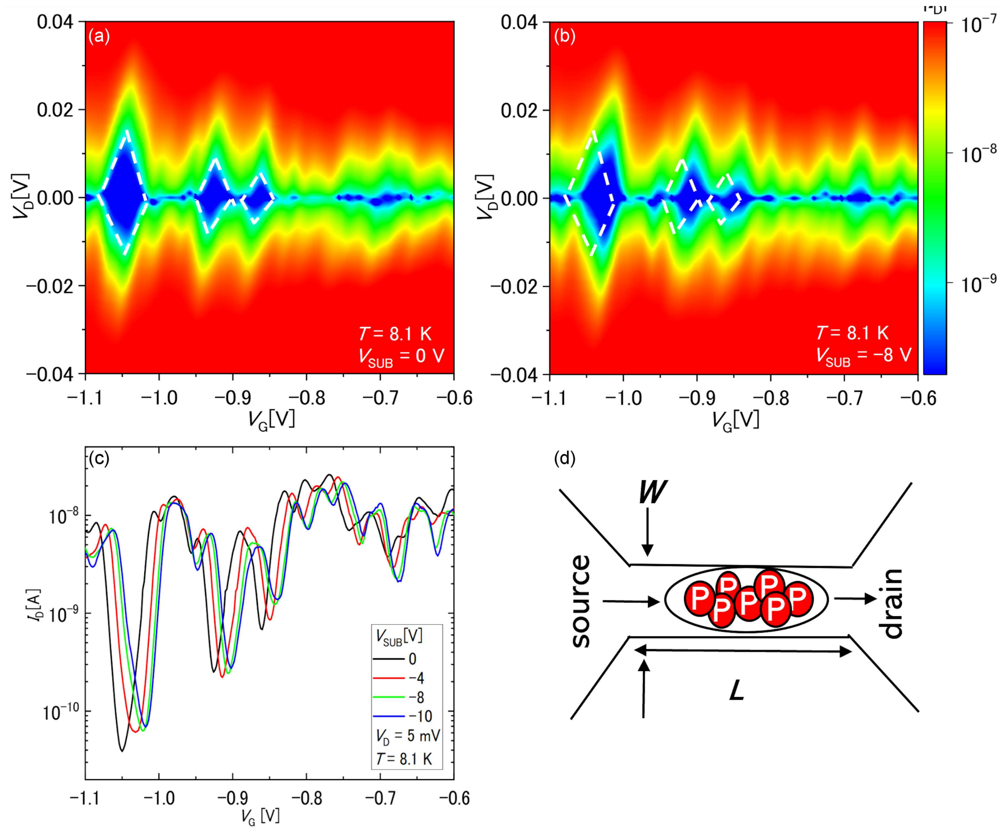

Fig. 2. (a)-(b) Stability diagrams at low temperature ($T = 8.1$ K) for an SOI-FET with a channel designed as a narrow point contact (designed dimensions: length $L = 0$ nm and width $W = 60$ nm). Two different values of the substrate voltage as a back gate ($V_{\mathrm{SUB}} = 0$ V in (a) and -8 V in (b)) are shown. (c) The I_{D}–V_{G} characteristics at different values of V_{SUB}. (d) A schematic illustration of a possible model (P-donor-induced single QD) that can explain the set of observed Coulomb diamonds.

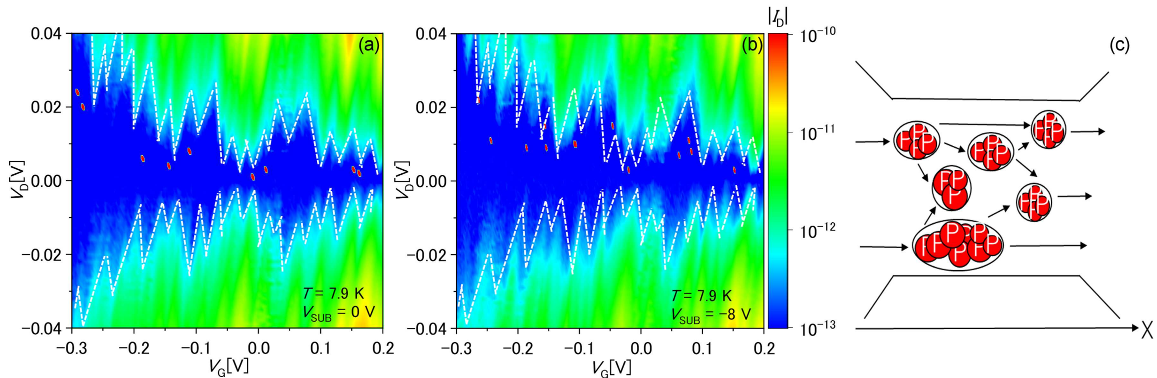

Fig. 3. (a)-(b) Stability diagrams at low temperature ($T = 7.9$ K) for an SOI-FET with the channel designed as a wide point contact (designed dimensions: length $L = 0$ nm and width $W = 200$ nm). Two different values of substrate voltage as a back gate ($V_{\mathrm{BG}} = 0$ and -8 V) are shown. (c) Schematic representation of a channel containing multiple P-donor-induced QDs.

a non-monotonous manner. Such behavior is typical for a more complex array of QDs (possibly containing multiple QDs in series and in parallel, hosted in the wider channel). When the edges of the diamonds are roughly delineated by dashed lines and transferred to the stability diagram obtained for more negative $V_{\mathrm{SUB}} = -8$ V, a similar shift of the features towards more positive V_{G} is found, as for the narrower device. This is, however, accompanied by more obvious changes of Coulomb diamonds, when compared to the narrower device shown in Fig. 2.

It is also seen that for small source-drain bias V_D, the current does not flow above the noise level of our measurements (typically 10–100 fA). The I_D–V_G characteristics clearly illustrate this situation. This suggests that Coulomb blockade is maintained up to higher V_D values for such arrays of QDs. These results suggest that a macroscopic control of channel dimensions (here, width) may allow statistical control of the number of QDs and of the complexity of the QD array. Studies of a larger number of such devices are necessary to provide a statistical overview.

It is also expected that such a complex QD array can be tuned with more ease by V_{SUB}. Therefore, to analyzing the behavior of the QD array found in the wider-channel SOI-FETs, a specific study is dedicated when V_{SUB} (i.e., vertical electric field) is changed systematically.

3. Discussion

Figure 4 presents, for the wider device with stability diagrams shown in Fig. 3, the contour plot of $|I_D|$ as a function of V_G and V_{SUB} by fixing $V_D = 5$ mV (for this case). Current peaks are observed as fine traces of non-noise-level current, stretching from top to bottom as V_{SUB} becomes more negative, thus increasing the vertical electric field. Such analysis was previously used to identify the coupling of single-donor QDs when the vertical electric field pushes the potential wells towards the Si/SiO_2 interface [17].

There are various types of behaviors noticeable in this contour plot, with sets of current-peak traces splitting or merging at different V_{SUB}, especially at higher V_G. However, here we focus on the features observed at the lowest values of V_G and, in particular, on the sudden changes marked by the white circles. These marks correspond to the disappearance of current peaks from roughly $V_{SUB} \approx -6$–-7 V and the reappearance of a different current peak from about $V_{SUB} \approx -14$ V.

A possible model to explain such peculiar behavior is illustrated in Fig. 4b, schematically depicting the existence of two different QDs near the front and, respectively, back interface (FI and BI, respectively), affected by the application of vertical electric field via V_{SUB}. It is possible that the current flows through both QDs for $V_{SUB} = 0$ V, changing significantly as V_{SUB} is applied in the negative direction, and eventually remaining controlled only by one QD (likely near the front interface) at the maximum values of V_{SUB} investigated here.

Although a more systematic analysis of experimental data, combined with simulations of dopant distributions, is necessary to fully confirm such a model, its plausibility is a reasonable consequence of the non-uniform distribution of dopants (dominantly P-donors remaining uncompensated by the B-acceptors). The fact that the SET current traces can be modulated by the application of an electric field is also promising for the development of functional devices in such nanoscale codoped SOI-FETs.

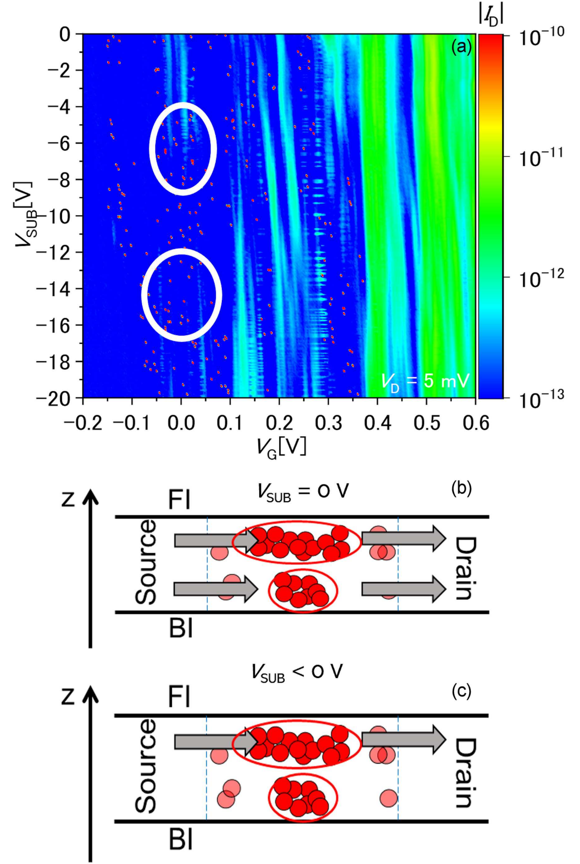

Fig. 4. (a) Effect of substrate voltage (V_{SUB}) on the fine traces of current (current peaks) taken as a function of V_G for small source-drain bias, $V_D = 5$ mV, at low temperature. Circles indicate positions at which current traces change significantly, suggesting a change of current paths between front interface (FI) and back interface (BI). (b)-(c) Two such schematics illustrating possible changes in SET current paths for different V_{SUB}.

4. Conclusions

This study focused on the analysis of the stability diagrams for two different devices, both silicon-on-insulator field-effect transistors (SOI-FETs) designed as point contacts ($L = 0$ nm), but with different designed widths ($W = 60$ and 200 nm, respectively). The stability diagram exhibits a simple set of distinct Coulomb diamonds for the narrowest SOI-FET, which is a signature of single-electron tunneling (SET) transport through a dominant-single-QD system. On the other hand, the stability

diagram for the wider SOI-FET exhibits a complex pattern of overlapping Coulomb diamonds, suggesting the presence of a more complex array of multiple QDs in the wider channel.

The effects of the vertical electric field, here controlled by additionally applying substrate voltage V_{SUB}, have also been investigated. Here, only data for the wider SOI-FET was shown, revealing how the SET-current traces are modified suddenly by the application of V_{SUB}. These results reflect the possibility of further control the nature of the QD array.

The specific effect of counter-doping by B-acceptors remains not fully clarified at this moment, requiring the fabrication of a series of samples where N_{A} is systematically changed as a parameter. Nevertheless, it is expected that a deeper understanding of the donor and acceptor distributions in such nanoscale SOI films can allow the design and optimization of SET devices with QDs formed by the random distribution of donors.

Acknowledgments

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References

[1] G. Moore, *Electronics Mag.* **38**, 114 (1965).

[2] A. Asenov, A.R. Brown, J.H. Davies, S. Kaya, G. Slavcheva, *IEEE Trans. Electron Devices* **50**, 1837 (1998).

[3] T. Skotnicki, J.A. Hutchby, T.-J. King, H.-S.P. Wong, F. Boeuf, *IEEE Circuits Devices Mag.* **21**, 16 (2005).

[4] *International Technology Roadmap for Semiconductors (ITRS)*, 2013.

[5] T. Shinada, S. Okamoto, T. Kobayashi, I. Ohdomari, *Nature* **437**, 1128 (2005).

[6] M. Fuechsle, J.A. Miwa, S. Mahapatra, H. Ryu, S. Lee, O. Warchkow, L.C.L. Hollenberg, G. Klimeck, M.Y. Simmons, *Nat. Nanotechnol.* **7**, 242 (2012).

[7] B. Weber, Y.H.M. Tan, S. Mahapatra, T.F. Watson, H. Ryu, R. Rahman, L.C.L. Hollenberg, G. Klimeck, M.Y. Simmons, *Nat. Nanotechnol.* **9**, 430 (2014).

[8] H. Sellier, G.P. Lansbergen, J. Caro, S. Rogge, N. Collaert, I. Ferain, M. Jurczak, S. Biesemans, *Phys. Rev. Lett.* **97**, 206805 (2006).

[9] Y. Ono, K. Nishiguchi, A. Fujiwara, H. Yamaguchi, H. Inokawa, Y. Takahashi, *Appl. Phys. Lett.* **90**, 102106 (2007).

[10] P.M. Koenraad, M.E. Flatté, *Nat. Mater.* **10**, 91 (2011).

[11] J.P. Colinge, C.W. Lee, A. Afzalian et al., *Nature Nanotechnol.* **5**, 225 (2010).

[12] J.P. Colinge, C.W. Lee, N.D. Akhavan, R. Yan, I. Ferain, P. Razavi, A. Kranti, R. Yu, in: *Semiconductor-On-Insulator Materials for Nanoelectronics Applications* Eds. A. Nazarov, J.P. Colinge, F. Balestra, J.P. Raskin, F. Gamiz, V. Lysenko, Springer, Berlin 2011.

[13] M. Tabe, D. Moraru, M. Ligowski, M. Anwar, R. Jablonski, Y. Ono, T. Mizuno, *Phys. Rev. Lett.* **105**, 016803 (2010).

[14] A. Udhiarto, D. Moraru, T. Mizuno, M. Tabe, *Appl. Phys. Lett.* **99**, 113108 (2011).

[15] E. Hamid, D. Moraru, Y. Kuzuya, T. Mizuno, L.T. Anh, H. Mizuta, M. Tabe, *Phys. Rev. B* **87**, 085420 (2013).

[16] D. Moraru, A. Samanta, L.T. Anh, T. Mizuno, H. Mizuta, M. Tabe, *Sci. Rep.* **4**, 6219 (2014).

[17] A. Samanta, D. Moraru, T. Mizuno, M. Tabe, *Sci. Rep.* **5**, 17377 (2015).

[18] A. Samanta, M. Muruganathan, M. Hori, Y. Ono, H. Mizuta, M. Tabe, D. Moraru, *Appl. Phys. Lett.* **110**, 093107 (2017).

[19] T.T. Jupalli, A. Debnath, G. Prabhudesai, K. Yamaguchi, P.J. Kumar, Y. Ono, D. Moraru, *Appl. Phys. Express* **15**, 065003 (2022).

[20] D. Moraru, T. Kaneko, Y. Tamura, T.T. Jupalli, R.S. Singh, C. Pandy, L. Popa, F. Iacomi, *Nanomaterials* **13**, 1911 (2023).

[21] C. Pandy, G. Prabhudesai, K. Yamaguchi, V.N. Ramakrishnan, Y. Neo, H. Mimura, D. Moraru, *Appl. Phys. Express* **14**, 055002 (2021).